WHAT IS CLAIMED IS:

1. An apparatus comprising:

a coreless substrate;

a layer of material attached to the substrate, the layer of material having a lower elastic modulus than the substrate;

an interposer coupled to the layer of material; and

a capacitive layer coupled to the interposer.

2. An apparatus according to Claim 1, further comprising:

an integrated circuit die coupled to the interposer.

3. An apparatus according to Claim 2, wherein the capacitive layer is disposed between the interposer and the integrated circuit die.

4. An apparatus according to Claim 1, further comprising:

a plurality of solder columns to couple the interposer to the substrate.

5. An apparatus according to Claim 4, the layer of material defining openings to pass the plurality of solder columns.

6. An apparatus according to Claim 4,

the interposer defining a plurality of vias to couple the plurality of solder columns to a plurality of solder balls,

further comprising an integrated circuit die coupled to the plurality of solder balls.

7. An apparatus according to Claim 1,

wherein the layer of material is laminated to the substrate.

8. An apparatus according to Claim 1, further comprising:

a stiffener attached to the layer of material.

9. An apparatus according to Claim 8, wherein the stiffener surrounds the interposer.

10. An apparatus according to Claim 1, wherein a first side of the interposer is coupled to the layer of material and the capacitor is coupled to a second side of the interposer.

11. A method comprising:

fabricating a coreless substrate;

attaching a layer of material to the substrate, the layer of material having a lower elastic modulus than the substrate; and

coupling an interposer having a capacitive layer to the layer of material.

12. A method according to Claim 11, further comprising:

fabricating solder columns within the layer of material.

13. A method according to Claim 12, wherein coupling the interposer to the layer of material comprises:

coupling the interposer to the solder columns.

14. A method according to Claim 12, further comprising:

fabricating a plurality of solder balls on the interposer, the interposer defining a plurality of vias to couple the plurality of solder columns to the plurality of solder balls.

15. A method according to Claim 14, further comprising:

coupling an integrated circuit die to the plurality of solder balls.

16. A method according to Claim 11, further comprising:

coupling an integrated circuit die to the interposer.

17. A method according to Claim 16, wherein coupling the integrated circuit die to the interposer comprises:

coupling the integrated circuit die to the capacitive layer.

18. A system comprising:

a microprocessor comprising:

a coreless substrate;

a layer of material attached to the substrate, the layer of material having a lower elastic modulus than the substrate;

an interposer coupled to the layer of material; and

a capacitive layer coupled to the interposer; and

a double data rate memory electrically coupled to the microprocessor.

19. A system according to Claim 18, further comprising:

an integrated circuit die coupled to the interposer.

20. A system according to Claim 19, wherein the capacitive layer is disposed between the interposer and the integrated circuit die.

21. A system according to Claim 18, further comprising:

a plurality of solder columns to couple the interposer to the substrate, the layer of material defining openings to pass the plurality of solder columns, and the interposer defining a plurality of vias to couple the plurality of solder columns to a plurality of solder balls; and

an integrated circuit die coupled to the plurality of solder balls.

22. A system according to Claim 18, further comprising:

a stiffener attached to the layer of material.

23. A system according to Claim 18, wherein a first side of the interposer is coupled to the layer of material and the capacitor is coupled to a second side of the interposer.

24. A system according to Claim 18, further comprising:

a motherboard electrically coupled to the microprocessor and to the memory.